PATENT ABSTRACTS OF JAPAN

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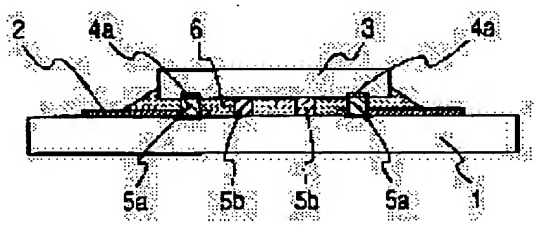
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To improve the mounting quality of a semiconductor chip in a semiconductor device.
SOLUTION: In a semiconductor device, an anisotropic conduction joint material 6, which electrically and mechanically connects a circuit electrode 2 and bumps 5a, is installed between the circuit electrode 2 formed on a circuit board 1 and a position facing the circuit electrode 2 at the lower face of a semiconductor chip 3. Dummy bumps 5b are formed in positions facing a part, where the circuit electrode of the circuit board 1 is not formed. When an application load to the semiconductor chip 3 for compressing and deforming the anisotripic conduction joint material 6 is set to a stable high load-side, the load is distributed to the dummy bumps 5b, and the circuit board 1 is prevented from being deformed and the circuit electrode 2 from being disconnected due to the application of excessive load.



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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to mounting to the circuit board of a semiconductor chip about a semiconductor device.
[0002]
[Description of the Prior Art] The trend of the mounting technology to the circuit board of a semiconductor chip in recent years is in the inclination of thin-shape[detailed-izing and]-izing in connection with a microminiaturization of electronic equipment, and densification. As the junction approach between a semiconductor chip and the circuit board, the anisotropy electric conduction junction which can perform detailed-izing and thin shape-ization rather than wirebonding from the former and soldering greatly attracts attention. After anisotropy electric conduction junction applies or sticks on the interior the anisotropy electric conduction jointing material for corrugated fibreboard which carried out homogeneity distribution of the conductive particle, it lays a semiconductor chip on this and performs pressurization of heating and the vertical direction to these in the predetermined semiconductor chip mounting position on the circuit board. While an anisotropy electric conduction jointing material for corrugated fibreboard is inserted between the bump formed in the inferior surface of tongue of a semiconductor chip, and the circuit electrode for flow connection formed in the edge in the middle of the circuit pattern of the circuit board, compresses and flows through between a bump and circuit electrodes by this by the electric conduction particle in this anisotropy electric conduction jointing material for corrugated fibreboard, an anisotropy electric conduction jointing material for corrugated fibreboard hardens with heating, and combines a semiconductor chip and the circuit board mechanically.
[0003] Although the substrate of the circuit board of the hard quality of the materials, such as a glass epoxy group plate of elastic-modulus 21GPa extent and a glass substrate, was common conventionally, the flexible substrate is also used by the appearance of thin semiconductor devices, such as an IC card, in recent years. The example of representation of an IC card is shown, the coil-like antenna pattern 73 is formed in circuit board 71 front face which constitutes one design sheet, and drawing 4 flows with the circuit electrode with which the semiconductor chip 74 mounted on the circuit board 73 was formed in the edge of an antenna pattern 73 by the bump who does not illustrate. On these, the design sheet 72 of another side is covered and it pastes up. In this IC card, what fabricated thinly the polyester (PET) resin of elastic-modulus 6GPa extent with which the circuit board 71 is supple in the shape of a sheet to about 0.1mm is used.
[0004] By the way, the mounting equipment of a semiconductor chip is constituted including the load impression equipment which impresses the load for pressurization to the top face of a semiconductor chip. In order to arrange the mounting quality of a semiconductor chip, it is desirable to use in the load field whose impression load the error rate of an impression load is small and is generally stable. In this case, in the thing of the hard quality of the materials, such as the conventional glass epoxy group plate, it is easy to obtain a positive flow by using the to some extent high load field by which an impression load is stabilized. however, the above — in the flexible circuit board, if the high load field by which an impression load is stabilized is used, as shown in drawing 5 , the bump 75 of the semiconductor chip 74 which a load concentrates eats into the circuit board 71, deformation of the circuit board 71 and an open circuit of the circuit electrode 731 will be caused, or junction endurance will fall. Although what is necessary is just to be newly able to develop mounting equipment to the circuit boards of the flexible quality of the material, while difficulty follows technically, even if it can do, facility costs increase. Moreover, it is necessary to make mounting Rhine of a semiconductor chip separate, and it cannot be admitted at all by the object for the circuit boards of the hard quality of the material, and the object for the circuit boards of the flexible quality of the material.
[0005] The back up plate, such as a copper foil, is prepared in the tooth back of the circuit board at which a semiconductor chip is not mounted, even if the circuit board deforms by load impression, what restored the variant part of the circuit board according to the elastic repulsive force of the back up plate is indicated after load discharge by JP,9-92683,A, and it is possible to mount the semiconductor chip in the Takani pile with the application of this technique.
[0006]
[Problem(s) to be Solved by the Invention] However, with a technique given [above-mentioned] in JP,9-92683,A, since 1 ** deforms the circuit board greatly by load impression, in case a variant part does not necessarily revert to satisfaction, but it performs design printing etc. to the inferior surface of tongue of the circuit board in an IC card etc. after mounting a semiconductor chip, it has a possibility that the effect of printing unevenness or a printing defect may appear. Moreover, the operation which once restores the disconnected circuit electrode is not necessarily done so.
[0007] This invention was made in view of the above-mentioned actual condition, and even if it impresses the Takani pile at the time of semiconductor chip mounting, it aims at offering the semiconductor device which can prevent deformation of the circuit board and a circuit electrode open circuit.
[0008]
[Means for Solving the Problem] A dummy bump is formed in the circuit electrode formed in the top face of the circuit

board on the inferior surface of tongue of a semiconductor chip, and the location which counters with the part of the circuit electrode agenesis of the above-mentioned circuit board in addition to the bump who forms in the location which counters in invention according to claim 1.

[0009] By preparing a dummy bump, in order to pressurize the anisotropy electric conduction jointing material for corrugated fibreboard interposed between the circuit board and a semiconductor chip, the load impressed to a semiconductor chip is distributed by the dummy bump, and an open circuit of deformation of the circuit board and the electrode of the circuit board can be prevented as an impression load is high. A deer is carried out and impression of the Takani pile with sufficient stability is attained.

[0010] The above-mentioned dummy bump is formed in the inspection pad front face of a semiconductor chip in invention according to claim 2.

[0011] Thereby, it cannot expose but the front face of an inspection pad can prevent the corrosion, after the membrane formation for bumps is made like other bump formation locations.

[0012] In invention according to claim 3, the above-mentioned circuit board is formed with the film made of resin, and the above-mentioned circuit electrode is formed with a conductive adhesion paste.

[0013] When the film made of resin which circuit board deformation tends to produce by the Takani pile impression, and the conductive adhesion paste which a circuit electrode open circuit tends to produce by the Takani pile impression are used, the greatest effectiveness which raises mounting quality can be acquired especially.

[0014]

[Embodiment of the Invention] Drawing 1 and drawing 2 explain the operation gestalt of the semiconductor device of this invention. Drawing 1 shows the mounting condition to the circuit board of a flip chip, and drawing 2 shows the bump who formed in the circuit side of a flip chip. The anisotropy electric conduction jointing-material-for-corrugated-fibreboard slack anisotropy electric conduction adhesive film 6 is formed in a flip chip mounting position at the circuit board 1, and the rectangular flip chip 3 is laid on it.

[0015] Bump 5a for flow connection has protruded on the inferior surface of tongue of a flip chip 3 on pad 4a which leads to the internal circuitry of a flip chip 3 formed in the four corners. Bump 5a for flow connection and the circuit electrode 2 formed in the circuit board 1 are formed so that it may counter mutually. Two have protruded at a time on the location which counters with the part of the electrode agenesis of the circuit board 1 apart from bump 5a for flow connection in dummy bump (suitably henceforth bump) 5b among drawing 2 on the inferior surface of tongue of a flip chip 3, respectively between bump 5a for both flow connection between bump 5a for both flow connection of a near side, and by the side of the back. The bumps 5a and 5b of a near side and the bumps 5a and 5b by the side of the back are stationed at abbreviation regular intervals, respectively.

[0016] Dummy bump 5b is formed together with this at the time of the bump 5a formation for flow connection. That is, in a wafer process, the heights of the metal which uses after formation and photograph RISOGURAI by a spatter etc., and becomes a bump formation location with a bump by plating or vacuum evaporationo alternatively about UBM (Under Bump Metal) film, such as (Titanium Ti)-chromium (Cr), are formed, after photoresist removal, selective etching of the UBM film of metal membrane agenesis is carried out, and Bumps 5a and 5b complete. Therefore, bump 5a for flow connection and dummy bump 5b have substantially the same height.

[0017] After laying each of bump 5a for flow connection which protruded from the inferior surface of tongue of a semiconductor chip 3, and dummy bump 5b on the anisotropy electric conduction adhesive film 6 by which temporary sticking by pressure was carried out at the circuit board 1, it presses lower anisotropy electric conduction adhesive film 6 grade by forcing the pressurization heating head of semiconductor chip mounting equipment on the top face of a semiconductor chip 3, and impressing a load. Since bump 5a for flow connection and dummy bump 5b have substantially the same height like the above, all the bumps 5a and 5b improves [balance] a pressure welding to the anisotropy electric conduction adhesive film 6. And the anisotropy electric conduction adhesive film 6 carries out the compression set only of the location across which it faced by the circuit board 1 and Bumps 5a and 5b in response to big welding pressure. This flows between the circuit electrode 2 of the circuit board 1, and bump 5a for flow connection. On the other hand, since dummy bump 5b does not counter with the circuit electrode 2 of the circuit board 1, the anisotropy electric conduction adhesive film 6 between the circuit board 1 and dummy bump 5b is not contributed to a flow.

[0018] Here, the impression load to a semiconductor chip 3 is distributed to four bumps 5for flow connection a, and four dummy bump 5b, and even if the impression load of mounting equipment is big, the load in each bumps 5a and 5b will not become big. In the example of drawing, since dummy bump 5b of the same number as bump 5a for flow connection is prepared, the load impressed to bump 5a for flow connection carries out an abbreviation reduction by half as compared with the conventional semiconductor device which does not have dummy bump 5b. A deer is carried out, it is prevented that the circuit board 1 deforms by bump 5a for flow connection, and, of course, as for deformation, the circuit board 1 does not produce dummy bump 5b, either. Moreover, when the circuit electrode 2 is also pressed by bump 5a for flow connection, even if it may dent to a circuit board 1 side, it is not generated and an open circuit does not spoil junction endurance with bump 5a for flow connection, either. A deer can be carried out and it can be compatible in setting the impression load by the pressurization heating head as a high value, and raising the stability of an impression load, and deformation of the circuit board 1 and prevention of an open circuit of the circuit electrode 2.

[0019] Next, mounting quality is evaluated about the example of this invention, and a result is explained. An example is what prepared bump 5a for flow connection, and every four dummy bump 5b for load distribution, respectively, as shown in drawing 2 , and the circuit board 1 formed the electrode in the PET sheet with a thickness of 100 micrometers by printing by the conductive adhesion paste. Each bumps 5a and 5b formed in 100micrometer** and height of 20 micrometers by golden (Au) plating. The anisotropy electric conduction film 6 used what blended the conductive particle with the sheet-like epoxy resin. And temporary sticking by pressure of the anisotropy electric conduction adhesive film 6 was carried out in the flip chip mounting position at the circuit board 1, the flip chip 3 was laid in piles so that the circuit electrode 2 of the circuit board 1 corresponding to a it top with bump 5a for flow connection might be in agreement, the load was impressed from on the flip chip 3 by the pressurization heating head in the condition, and this sticking by pressure was

performed. Temporary sticking by pressure was performed on 80-degreeC, 200gf / chip, and the conditions for 3 seconds, and this continuing sticking by pressure was performed on 190-degreeC, 500gf / chip, and the conditions for 20 seconds. In addition, this above-mentioned sticking-by-pressure load is the value of the load field by which a load is stabilized in semiconductor chip mounting equipment.

[0020] On the other hand, except for the point that a dummy bump is agenesis, the thing of the same specification as an example was prepared as an example of a comparison.

[0021] The quality evaluation result about an example and the example of a comparison is shown in Table 1. In the example, such fault was not generated to cutting of a circuit electrode and deformation of the circuit board having arisen in the example of a comparison. Moreover, in addition, conductivity was good about junction endurance 1000 hours or more after [example] to defective continuity having occurred under 70 degrees of ambient temperature C in the example of a comparison in 850 hours.

[0022]

[Table 1]

	比較例 (ダミーバンプなし)	実施例 (ダミーバンプあり)
実装荷重	500gf／チップ	←
接合状態	・回路電極の切断 ・回路基板の変形	接合状態良好
接合耐久性	70℃×850hrにて 導通不良発生	70℃×1000hr以上で 導通性良好

[0023] Thus, by this invention, by preparing the dummy bump who makes a load distribute, even if it is a semiconductor device using the flexible circuit boards, such as an IC card, mounting by the Takani pile by which an impression load is stabilized is attained. Here, since a dummy bump is formed together with the bump for flow connection like the above, she can respond only by modification of the photo mask for bump formation. Therefore, it is not necessary to newly introduce semiconductor chip mounting equipment, and mounting Rhine is not depended on the class of quality of the material of the circuit board, but can be constituted in common.

[0024] In addition, a dummy bump's installation location, a configuration, a number, etc. make [many] the number of dummy bumps, so that there are few bumps for flow connection like the flip chip by which it is good to choose suitably according to the setting load demanded according to the load stability of mounting equipment etc., for example, it is used for an IC card, and the impression load according to load stability demanded is high. Moreover, a dummy bump's formation location is good for the inferior surface of tongue of a semiconductor chip to arrange as equally as possible. In addition, a dummy bump does not necessarily need to be among the bumps for flow connection.

[0025] Moreover, dummy bump 5b is also good to establish some or all of them in the front face of checking pad 4b which is formed in the inferior surface of tongue of a semiconductor chip 3 apart from pad 4a, and is used for the performance verification of a semiconductor chip 3, as shown in drawing 3 . In this case, the following effectiveness is done so. That is, in what does not form a bump in a checking pad, a front face will expose a checking pad by carrying out etching removal of the UBM film at the time of the above-mentioned bump formation. Since the aluminum which is usually inferior to Au used for a bump in corrosion resistance is used, there is a possibility of receiving a damage in etching of the UBM film, a subsequent washing process, etc., and bringing about corrosion in a checking pad. On the other hand, in what formed the dummy bump in the checking pad, after formation of the above-mentioned UBM film, since the front face of checking pad 4b is not exposed, it can prevent the corrosion of checking pad 4b.

[0026] Moreover, a liquefied thing is also easy to be natural although the anisotropy electric conduction adhesive film is used as an anisotropy electric conduction jointing material for corrugated fibreboard.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the semiconductor chip mounting condition of the semiconductor device of this invention.
[Drawing 2] It is a perspective view by the side of the inferior surface of tongue of the semiconductor chip of the semiconductor device of this invention.
[Drawing 3] It is drawing showing the semiconductor chip mounting condition of the modification of the semiconductor device of this invention.
[Drawing 4] It is the decomposition perspective view of the example of representation of an IC card.
[Drawing 5] It is drawing showing the example of representation of the semiconductor chip mounting condition of the conventional semiconductor device.
[Description of Notations]
1 Circuit Board
2 Circuit Electrode
3 Semiconductor Chip
4b A checking pad
5a Bump
5b Dummy bump
6 Anisotropy Electric Conduction Adhesive Film (Anisotropy Electric Conduction Jointing Material for Corrugated Fibreboard)

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by to form a dummy bump in the part of the circuit electrode agenesis of the above-mentioned circuit board, and the location which counters on the inferior surface of tongue of the above-mentioned semiconductor chip in the semiconductor device which interposed the anisotropy electric-conduction jointing material for corrugated fibreboard to which these are made to join electrically and mechanically between the circuit electrode formed in the top face of the circuit board, the above-mentioned circuit electrode of a semiconductor chip, and the bump who formed in the location which counters.
[Claim 2] The semiconductor device which formed the above-mentioned dummy bump in the inspection pad front face of a semiconductor chip in the semiconductor device according to claim 1.
[Claim 3] Claim 1 or the semiconductor device which formed the above-mentioned circuit board with the film made of resin, and formed the above-mentioned circuit electrode with a conductive adhesion paste in the semiconductor device of a publication 2 either.

[Translation done.]

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審査請求　有　　請求項の数３　ＯＬ　（全　５　頁）

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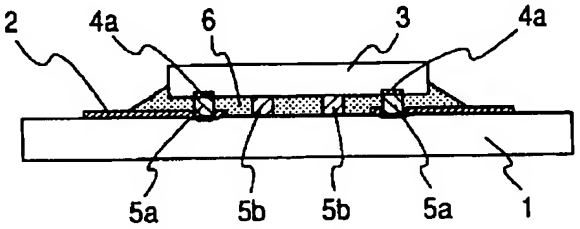
(54)【発明の名称】　半導体装置

(57)【要約】
【課題】　半導体装置において半導体チップの実装品質を高めることである。
【解決手段】　回路基板１の上面に形成した回路電極２と、半導体チップ３の下面に回路電極２と対向する位置に形成したバンプ５ａとの間に、これらを電気的かつ機械的に結合せしめる異方性導電接合材６を介設した半導体装置において、半導体チップ３の下面に、回路基板１の回路電極非形成の部位と対向する位置に、ダミーバンプ５ｂを形成することで、異方性導電接合材６を圧縮、変形せしめるための半導体チップ３への印加荷重を、安定性のよい高荷重側に設定したときに、その荷重がダミーバンプ５ｂに分散するようにし、過剰な荷重印加で回路基板１が変形したり回路電極２が断線しないようにする。



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【特許請求の範囲】

【請求項１】　回路基板の上面に形成した回路電極と、半導体チップの上記回路電極と対向する位置に形成したバンプとの間に、これらを電気的かつ機械的に接合せしめる異方性導電接合材を介設した半導体装置において、上記半導体チップの下面には、上記回路基板の回路電極非形成の部位と対向する位置に、ダミーバンプを形成したことを特徴とする半導体装置。

【請求項２】　請求項１記載の半導体装置において、上記ダミーバンプを半導体チップの検査パッド表面に形成した半導体装置。

【請求項３】　請求項１または２いずれか記載の半導体装置において、上記回路基板を樹脂製フィルムにより形成し、上記回路電極を導電性接着ペーストにより形成した半導体装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体装置に関し、特に半導体チップの回路基板への実装に関する。

【０００２】

【従来の技術】近年の半導体チップの回路基板への実装技術の動向は、電子機器の超小型化、高密度化に伴い、微細化、薄型化の傾向にある。半導体チップと回路基板との間の接合方法として、従来からのワイヤボンディング、はんだ付けよりも微細化、薄型化のできる異方性導電接合が大いに注目されている。異方性導電接合は、回路基板上の所定の半導体チップ実装位置に、内部に導電性粒子を均一分散させた異方性導電接合材を塗布又は貼付けした後、この上に半導体チップを載置し、これらに加熱および上下方向の加圧を行うものである。これにより、異方性導電接合材が、半導体チップの下面に形成されたバンプと、回路基板の回路パターンの途中または端部に形成された導通接続用の回路電極との間に挟まれ圧縮して、この異方性導電接合材中の導電粒子によりバンプと回路電極の間を導通するとともに、異方性導電接合材が加熱により硬化して半導体チップと回路基板とを機械的に結合する。

【０００３】回路基板は、従来、弾性率２１ＧＰａ程度のガラスエポキシ基板やガラス基板等の硬い材質の基板が一般的であったが、近年、ＩＣカード等の薄型の半導体装置の登場により柔軟な基板も用いられている。図４はＩＣカードの代表例を示すもので、一方の意匠シートを構成する回路基板７１表面には巻線状のアンテナパターン７３が形成され、回路基板７３上に実装された半導体チップ７４が、図示しないバンプにてアンテナパターン７３の端部に形成された回路電極と導通する。これらの上には他方の意匠シート７２が被覆、接着される。かかるＩＣカード等では、回路基板７１は柔軟性のある弾性率６ＧＰａ程度のポリエステル（ＰＥＴ）樹脂等を０．１ｍｍ程度に薄くシート状に成形したものが用いられる。

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【０００４】ところで、半導体チップの実装装置は、半導体チップの上面に加圧用の荷重を印加する荷重印加装置を含み構成されている。半導体チップの実装品質を揃えるには、一般に印加荷重の誤差割合が小さく印加荷重が安定している荷重領域で用いるのが望ましい。この場合、従来のガラスエポキシ基板等の硬い材質のものでは、印加荷重が安定するある程度高い荷重領域を用いることで、確実な導通を得ることが容易である。しかしながら、上記柔軟な回路基板では、印加荷重が安定する高い荷重領域を用いると、図５に示すように、荷重が集中する半導体チップ７４のバンプ７５が回路基板７１に食い込み、回路基板７１の変形や回路電極７３１の断線を引き起こしたり、接合耐久性が低下する。柔軟な材質の回路基板用に実装装置を新たに開発できればよいが、技術的に困難が伴うとともに、できたとしても設備費用が嵩む。また、半導体チップの実装ラインを硬い材質の回路基板用と柔軟な材質の回路基板用とで別々にする必要があり、到底容認できない。

【０００５】特開平９－９２６８３号公報には、半導体チップが実装されない回路基板の背面に銅泊等の補強板を設けて、荷重印加により回路基板が変形しても荷重解除後に補強板の弾性反発力により回路基板の変形部を復元するようにしたものが記載されており、この技術を適用して高荷重での半導体チップの実装を行うことが考えられる。

【０００６】

【発明が解決しようとする課題】しかしながら、上記特開平９－９２６８３号公報記載の技術では、回路基板は荷重印加により一旦は大きく変形するから、変形部が必ずしも満足に復元せず、ＩＣカード等において半導体チップを実装後に回路基板の下面に意匠印刷等を施す際に印刷むらや印刷欠陥の影響が現れるおそれがある。また、一旦、断線した回路電極を修復する作用を奏するわけではない。

【０００７】本発明は上記実情に鑑みなされたもので、半導体チップ実装時に高荷重を印加しても回路基板の変形や回路電極断線を防止することのできる半導体装置を提供することを目的とする。

【０００８】

【課題を解決するための手段】請求項１記載の発明では、半導体チップの下面に、回路基板の上面に形成した回路電極と対向する位置に形成するバンプに加え、上記回路基板の回路電極非形成の部位と対向する位置にダミーバンプを形成する。

【０００９】ダミーバンプを設けることにより、回路基板と半導体チップ間に介設される異方性導電接合材を加圧するために半導体チップに印加される荷重がダミーバンプに分散され、印加荷重が高くとも回路基板の変形や回路基板の電極の断線を防止することができる。しかし

て安定性のよい高荷重の印加が可能となる。

【００１０】請求項２記載の発明では、上記ダミーバンプを半導体チップの検査パッド表面に形成する。

【００１１】これにより、検査パッドの表面は、他のバンプ形成位置と同様にバンプ用の成膜がなされた後、露出せず、その腐食を防止することができる。

【００１２】請求項３記載の発明では、上記回路基板を樹脂製フィルムにより形成し、上記回路電極を導電性接着ペーストにより形成する。

【００１３】高荷重印加により回路基板変形が生じやすい樹脂製フィルム、および高荷重印加により回路電極断線が生じやすい導電性接着ペーストを用いたときに、実装品質を高める特に絶大な効果を得ることができる。

【００１４】

【発明の実施の形態】本発明の半導体装置の実施形態を、図１、図２により説明する。図１はフリップチップの回路基板への実装状態を示し、図２はフリップチップの回路面に形成したバンプを示している。回路基板１にはフリップチップ実装位置に異方性導電接合材たる異方性導電接着フィルム６が設けられ、その上に矩形のフリップチップ３が載置してある。

【００１５】フリップチップ３の下面には、その四隅に形成された、フリップチップ３の内部回路に通じるパッド４ａ上に導通接続用のバンプ５ａが突設してある。導通接続用バンプ５ａと回路基板１に形成した回路電極２とは互いに対向するように形成される。フリップチップ３の下面には、導通接続用バンプ５ａとは別に、回路基板１の電極非形成の部位と対向する位置に、図２中、手前側の両導通接続用バンプ５ａの間、および奥側の両導通接続用バンプ５ａの間に、それぞれ２つづつダミーバンプ（以下、適宜バンプともいう）５ｂが突設してある。手前側のバンプ５ａ，５ｂおよび奥側のバンプ５ａ，５ｂは、それぞれ略等間隔に配置される。

【００１６】ダミーバンプ５ｂは導通接続用バンプ５ａ形成時に、これと一緒に形成される。すなわち、ウェハプロセスにおいて、チタン（Ｔｉ）－クロム（Ｃｒ）等のＵＢＭ（Ｕｎｄｅｒ　Ｂｕｍｐ　Ｍｅｔａｌ）膜をスパッタ等により形成後、フォトリソグラィーを援用してバンプ形成位置に選択的に、メッキや蒸着によりバンプとなる金属の凸部を形成し、フォトレジスト除去後、金属膜非形成のＵＢＭ膜を選択エッチングしてバンプ５ａ，５ｂが完成する。したがって導通接続用バンプ５ａとダミーバンプ５ｂとは高さが実質的に同じである。

【００１７】半導体チップ３の下面から突設された導通接続用バンプ５ａとダミーバンプ５ｂとは、いずれも、回路基板１に仮圧着された異方性導電接着フィルム６上に載置した後、半導体チップ実装装置の加圧加熱ヘッドを半導体チップ３の上面に押し付けて荷重を印加することにより、下側の異方性導電接着フィルム６等を押圧する。上記のごとく、導通接続用バンプ５ａとダミーバンプ５ｂとは高さが実質的に同じであるから、すべてのバンプ５ａ，５ｂがバランスよく異方性導電接着フィルム６と圧接する。そして、異方性導電接着フィルム６は回路基板１とバンプ５ａ，５ｂとで挟まれた位置のみ大きな加圧力を受けて圧縮変形する。これにより、回路基板１の回路電極２と導通接続用のバンプ５ａとの間は導通する。一方、ダミーバンプ５ｂは回路基板１の回路電極２と非対向であるから、回路基板１とダミーバンプ５ｂとの間の異方性導電接着フィルム６は導通には寄与しない。

【００１８】ここで、半導体チップ３への印加荷重は４つの導通接続用バンプ５ａ、４つのダミーバンプ５ｂに分散し、実装装置の印加荷重が大きなものであっても、各バンプ５ａ，５ｂにおける荷重は大きなものにはならない。図例では導通接続用バンプ５ａと同じ数のダミーバンプ５ｂが設けてあるから、導通接続用バンプ５ａに印加される荷重は、ダミーバンプ５ｂを有しない従来の半導体装置に比して略半減する。しかして、導通接続用バンプ５ａにより回路基板１が変形することが防止され、勿論、ダミーバンプ５ｂでも回路基板１が変形は生じない。また、回路電極２も導通接続用バンプ５ａにより押圧されることにより回路基板１側へ凹むことはあっても断線は生じず、導通接続用バンプ５ａとの接合耐久性も損なうことはない。しかして、加圧加熱ヘッドによる印加荷重を高い値に設定して印加荷重の安定性を高めることと、回路基板１の変形や回路電極２の断線の防止とを両立することができる。

【００１９】次に本発明の実施例について実装品質を評価して結果について説明する。実施例は、図２に示すように導通接続用バンプ５ａと、荷重分散用のダミーバンプ５ｂとをそれぞれ４つずつ設けたもので、回路基板１は厚さ１００μｍのＰＥＴ樹脂シートに導電性接着ペーストによる印刷で電極を形成した。各バンプ５ａ，５ｂは金（Ａｕ）メッキにより１００μｍ□、高さ２０μｍに形成した。異方性導電フィルム６はシート状エポキシ樹脂に導電性粒子を配合したものを用いた。そして、回路基板１にはフリップチップ実装位置に異方性導電接着フィルム６を仮圧着し、その上にフリップチップ３を、導通接続用バンプ５ａと、対応する回路基板１の回路電極２とが一致するように重ねて載置し、その状態で加圧加熱ヘッドによりフリップチップ３の上から荷重を印加して本圧着をおこなった。仮圧着は８０°Ｃ、２００ｇｆ／チップ、３秒の条件で行い、続く本圧着は１９０°Ｃ、５００ｇｆ／チップ、２０秒の条件で行った。なお、上記本圧着荷重は半導体チップ実装装置において、荷重が安定する荷重領域の値である。

【００２０】一方、比較例として、ダミーバンプが非形成である点を除き実施例と同じ仕様のものを用意した。

【００２１】表１に実施例および比較例についての品質評価結果を示す。比較例では、回路電極の切断や回路基

板の変形が生じたのに対して、実施例ではこのような不具合は発生しなかった。また、接合耐久性については、比較例では雰囲気温度７０°Ｃのもとで８５０時間で導通不良が発生したのに対して、実施例では１０００時間＊＊以上を経てなお導通性は良好であった。

【００２２】

【表１】

	比較例（ダミーバンプなし）	実施例（ダミーバンプあり）
実装荷重	500gf／チップ	←
接合状態	・回路電極の切断 ・回路基板の変形	接合状態良好
接合耐久性	70℃×850hrにて導通不良発生	70℃×1000hr以上で導通性良好

【００２３】このように、本発明では荷重を分散せしめるダミーバンプを設けることで、ＩＣカード等の柔軟な回路基板を用いる半導体装置であっても、印加荷重が安定する高荷重での実装が可能となる。ここで、ダミーバンプは上記のごとく、導通接続用バンプと一緒に形成されるから、バンプ形成用のフォトマスクの変更のみで対応することができる。したがって、半導体チップ実装装置を新たに導入する必要もなく、実装ラインを回路基板の材質の種類によらず共通に構成できる。

【００２４】なお、ダミーバンプの設置位置、形状、数等は、実装装置の荷重安定性等に応じて要求される設定荷重により適宜選択するのがよく、例えば、ＩＣカードに用いられるフリップチップのように導通接続用のバンプの数が少ないほど、荷重安定性に応じた要求される印加荷重が高いほどダミーバンプの数を多くする。また、ダミーバンプの形成位置は、半導体チップの下面にできるだけ均等に配置するのがよい。なおダミーバンプは必ずしも導通接続用のバンプの間にある必要はない。

【００２５】また、ダミーバンプ５ｂはそのうちの一部もしくは全部を、図３に示すように、半導体チップ３の下面に、パッド４ａとは別に形成されて半導体チップ３の性能検査に用いられる検査用のパッド４ｂの表面に設けるのもよい。この場合、次の効果を奏する。すなわち、検査用パッドにバンプを形成しないものでは、検査用パッドは、上記バンプ形成時にＵＢＭ膜がエッチング除去されることにより表面が露出することになる。検査用パッドには、通常、バンプに用いるＡｕ等よりも耐蝕性が劣るアルミニウム等が用いられるから、ＵＢＭ膜のエッチングやその後の洗浄工程等においてダメージを受け腐食をもたらすおそれがある。これに対して検査用パッドにダミーバンプを形成したものでは、検査用パッド４ｂの表面が上記ＵＢＭ膜の形成後、露出することがないから、検査用パッド４ｂの腐食を防止することができる。

【００２６】また、異方性導電接合材として異方性導電接着フィルムを用いているが、液状のものでも勿論よい。

【図面の簡単な説明】

【図１】本発明の半導体装置の半導体チップ実装状態を示す図である。

【図２】本発明の半導体装置の半導体チップの下面側の斜視図である。

【図３】本発明の半導体装置の変形例の半導体チップ実装状態を示す図である。

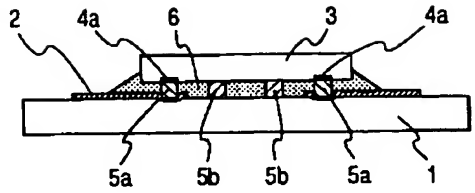
【図４】ＩＣカードの代表例の分解斜視図である。

【図５】従来の半導体装置の半導体チップ実装状態の代表例を示す図である。

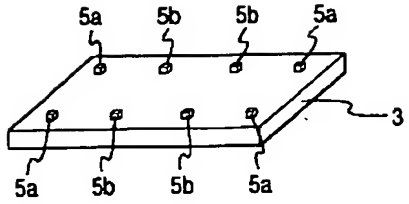
【符号の説明】

１　回路基板
２　回路電極
３　半導体チップ
４ｂ　検査用のパッド
５ａ　バンプ
５ｂ　ダミーバンプ
６　異方性導電接着フィルム（異方性導電接合材）

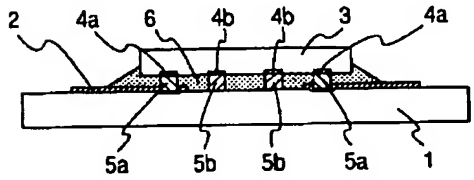
【図１】



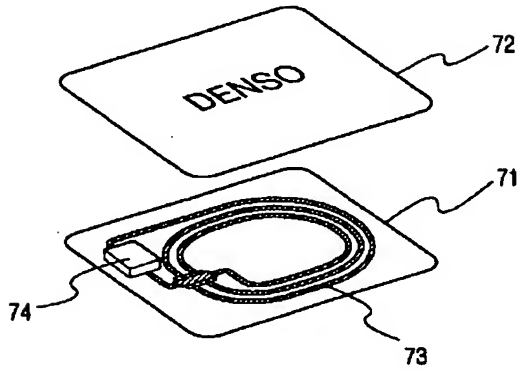
【図２】



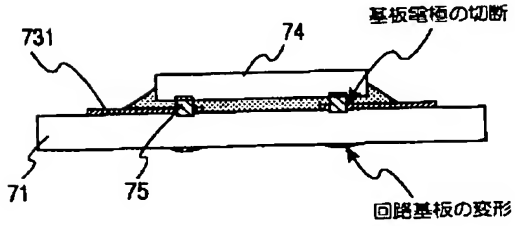
【図３】



【図４】



【図５】



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